AMENDMENTS

Please amend claims 8, 12, 21, 25, 29 and 34 to read as follows:

8. (Twice Amended) A lamination ceramic chip inductor, comprising at least one conductive pattern, the at least one fine, continuous conductive pattern having a thickness of 10 μm or more and a width to thickness ratio from 1 to less than 5.

12. (Twice Amended) A lamination ceramic chip inductor, comprising at least one fine, continuous conductive pattern formed by an electroforming process using a photoresist, the at least one conductive pattern having a thickness of 10 μm or more and a width to thickness ratio from 1 to less than 5.

21. (Amended) A lamination ceramic chip inductor, comprising at least one fine, continuous conductive pattern formed between at least one pair of insulation layers so as to have no specific gap between the at least one conductive pattern and the at least one pair of insulation layers, the at least one conductive pattern having a thickness of 10 μm or more and a width to thickness ratio from 1 to less than 5.

25. (Amended) A lamination ceramic chip inductor, comprising at least one fine, continuous conductive pattern formed by an electroforming process using a photoresist, the at least one conductive pattern having a thickness of 10 μm or more and a width to thickness ratio from 1 to less than 5,

wherein the at least one conductive pattern is formed between at least one pair of insulation layers so as to have no specific gap therebetween.

29. (Amended) A lamination ceramic chip inductor, comprising at least one conductive pattern formed between at least one pair of insulation layers so as to have no specific gap between the at least one conductive pattern and the at least one pair of insulation layers, the at least one conductive pattern consisting of metal selected from the group consisting of Ag, Au, Pt, Pd, Cu, Ni and alloys thereof.

34. (Amended) A lamination ceramic chip inductor, comprising at least one conductive pattern formed by an electroforming process using a photoresist, wherein the at least one conductive pattern is formed between at least one pair of insulation layers so as to have no specific gap therebetween, the at least one conductive pattern consisting of metal selected from the group consisting of Ag, Au, Pt, Pd, Cu, Ni and alloys thereof.

A version of the above amended claims marked to indicate the specific amendments may be found in the attached Appendix, in accordance with 37 CFR 1.121(c)(1).

Please add the following new claims:

39. (New) A lamination ceramic chip inductor, according to claim 8, wherein the conductive pattern has edges which are not blurred.

40. (New) A lamination ceramic chip inductor, according to claim 11, wherein the at least one pair of magnetic insulation layers are sintered, and the conductive pattern is surrounded by the sintered magnetic layers with a high density and no specific gap between the conductive pattern and the magnetic layers.

41. (New) A lamination ceramic chip inductor, according to claim 12, wherein the conductive pattern has edges which are not blurred.

42. (New) A lamination ceramic chip inductor, according to claim 15, wherein the at least one pair of magnetic insulation layers are sintered, and the conductive pattern is surrounded by the sintered magnetic layers with a high density and no specific gap between the conductive pattern and the magnetic layers.

43. (New) A lamination ceramic chip inductor, according to claim 21, wherein the conductive pattern has edges which are not blurred.

44. (New) A lamination ceramic chip inductor, according to claim 24, wherein the at least one pair of magnetic insulation layers are sintered, and the conductive pattern is surrounded by the sintered magnetic layers with a high density as a result of the no specific gap between the conductive pattern and the magnetic layers.

45. (New) A lamination ceramic chip inductor, according to claim 25, wherein the conductive pattern has edges which are not blurred.

46. (New) A lamination ceramic chip inductor, according to claim 28, wherein the at least one pair of magnetic insulation layers are sintered, and the conductive pattern is surrounded by the sintered magnetic layers with a high density as a result of the no specific gap between the conductive pattern and the magnetic layers.

47. (New) A lamination ceramic chip inductor, according to claim 29, wherein the conductive pattern has edges which are not blurred.

48. (New) A lamination ceramic chip inductor, according to claim 32, wherein the at least one pair of magnetic insulation layers are sintered, and the